

FH8812

N-Channel Enhancement Mode MOSFET

Description

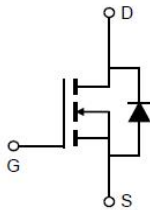
The FH8812 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and high density cell Design for ultra low on resistance. This device is suitable for use as a load switch or in PWM applications.

Application

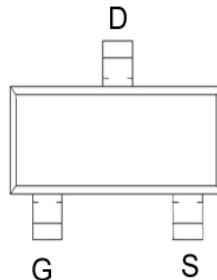
- ◆ PWM applications
- ◆ Load switch

General Features

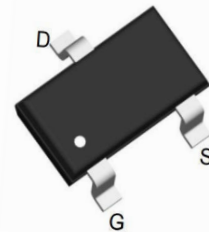
- ◆ $V_{DS} = 20V$, $I_D = 8.2A$
- ◆ $R_{DS(ON)}(Typ.) = 9.4m\Omega$ @ $V_{GS} = 4.5V$
- ◆ $R_{DS(ON)}(Typ.) = 11m\Omega$ @ $V_{GS} = 2.5V$
- ◆ High power and current handing capability
- ◆ Lead free product is acquired
- ◆ Surface mount package
- ◆ Fast Switching



Schematic diagram



Marking and Pin Assignment



SOT-23-3L top view

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

parameter	symbol	limit	unit
Drain-source voltage	V_{DS}	20	V
Gate-source voltage	V_{GS}	± 12	V
Continuous Drain Current	I_D	8.2	A
Pulsed Drain Current (Note 3)	I_{DM}	33	A
Drain-source Diode forward current (Note 1)	I_S	3	A
Maximum power dissipation	P_D	1.25	W
Operating junction Temperature range	T_j	-55 – 150	°C

Thermal Characteristics

Thermal Resistance junction-to ambient (Note 3)	Rth JA	100	°CW
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■ Electrical Characteristics (T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Drain-source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	0.5	0.7	0.9	V
Gate-Body Leakage Current	I _{GSS}	V _{DS} = 0V, V _{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20V, V _{GS} = 0V			1	μA
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 4.5V, I _D = 6.0A		9.4	12	mΩ
		V _{GS} = 2.5V, I _D = 4.0A		11	15	
Forward Transconductance	g _{FS}	V _{DS} = 5V, I _D = 5.0A		11		S
Diode Forward Voltage (Note 2)	V _{SD}	V _{GS} = 0V, I _S = 3A			1.2	V
Diode Forward Current (Note 1)	I _S				3	A
Dynamic						
Total Gate Charge	Q _g	V _{DS} = 10V, V _{GS} = 4.5V, I _D = 3A		12.0		nC
Gate-Source Charge	Q _{gs}			1.3		
Gate-Drain Charge	Q _{gd}			18		
Input Capacitance	C _{iss}	V _{DS} = 10V, V _{GS} = 0V, f = 1MHz		1150		pF
Output Capacitance	C _{oss}			188		
Reverse Transfer Capacitance	C _{rss}			167		
Switching						
Turn-On Delay Time	t _{d(on)}	V _{DS} = 10V, R _L = 5Ω, V _{GS} = 4.5V, R _{GEN} = 6Ω, I _D = 1A		13		nS
Rise Time	t _r			3.3		
Turn-Off Delay Time	t _{d(off)}			29.3		
Fall-Time	t _f			3.4		

Note: 1. Mounted on FR4 board, t ≤ 10sec.

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

3. Repetitive Rating: Pulse width limited by maximum junction temperature.

Typical Performance Characteristics

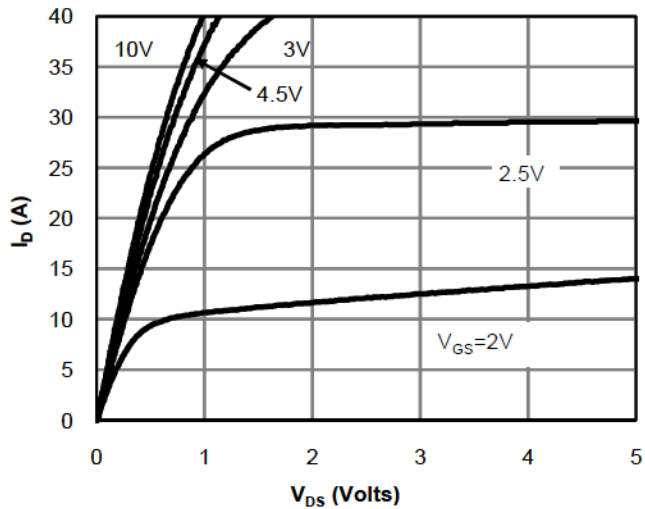


Fig 1: On-Region Characteristics (Note E)

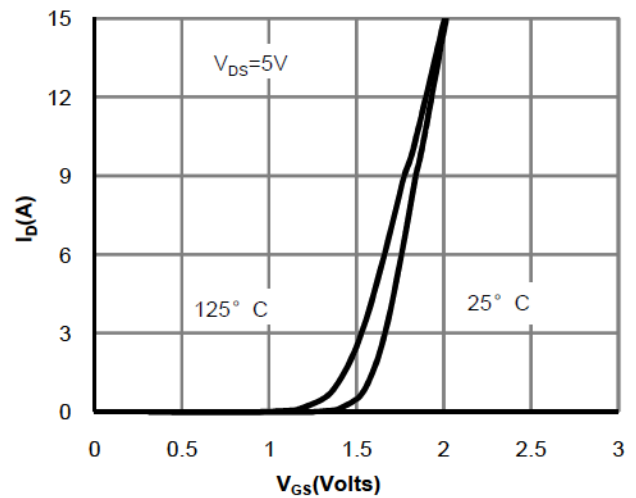


Figure 2: Transfer Characteristics (Note E)

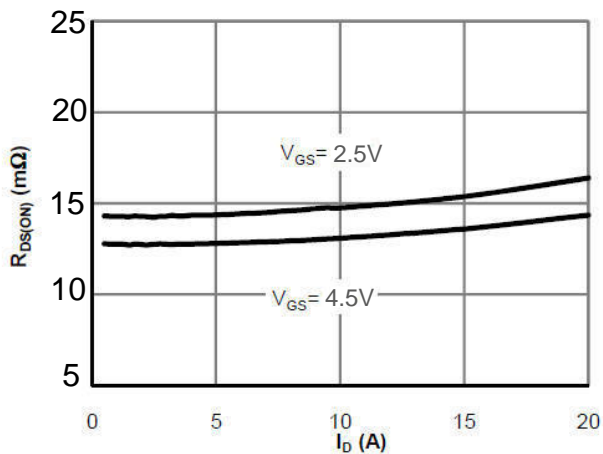


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

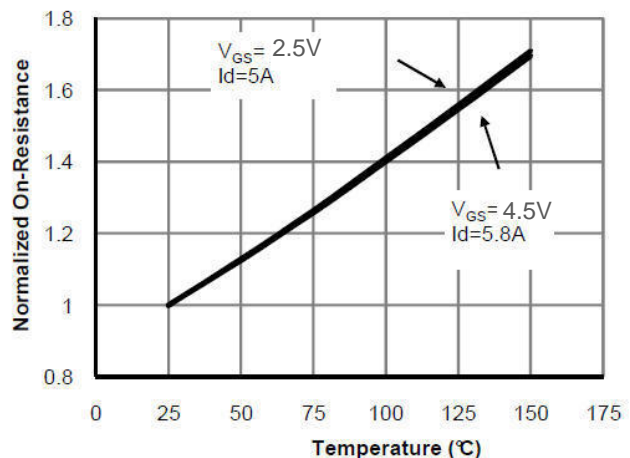


Figure 4: On-Resistance vs. Junction Temperature (Note E)

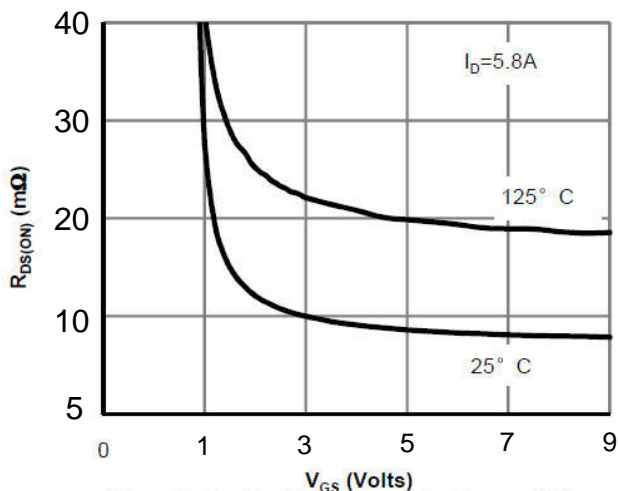


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

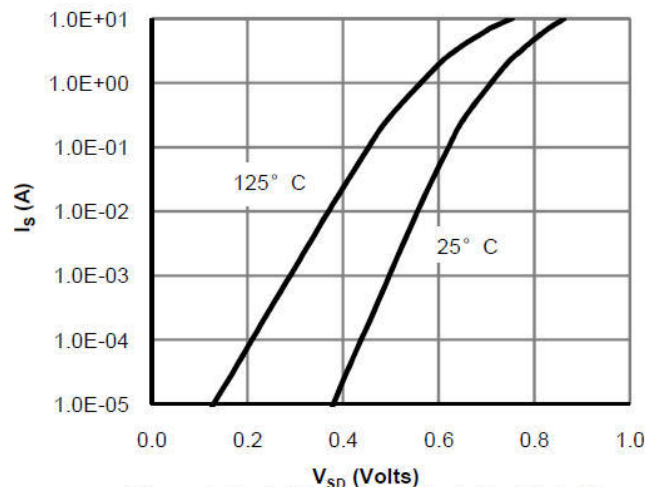


Figure 6: Body-Diode Characteristics (Note E)

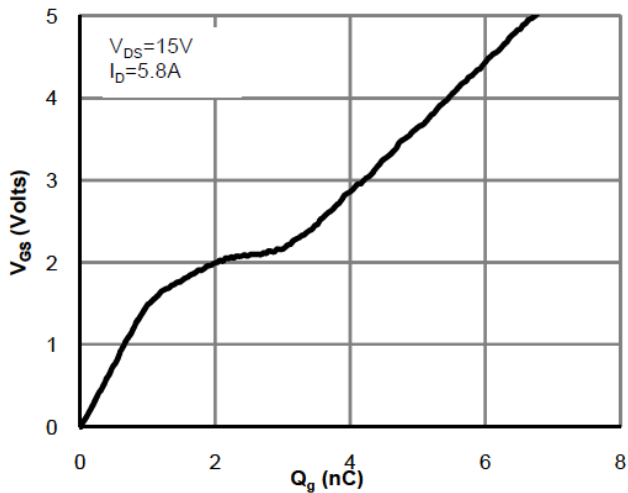


Figure 7: Gate-Charge Characteristics

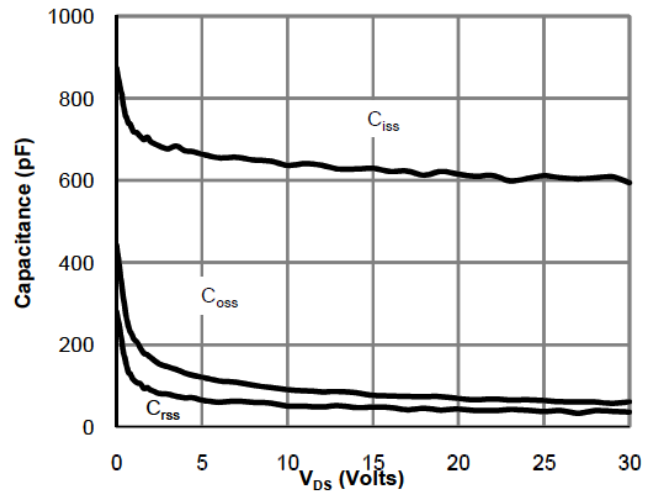


Figure 8: Capacitance Characteristics

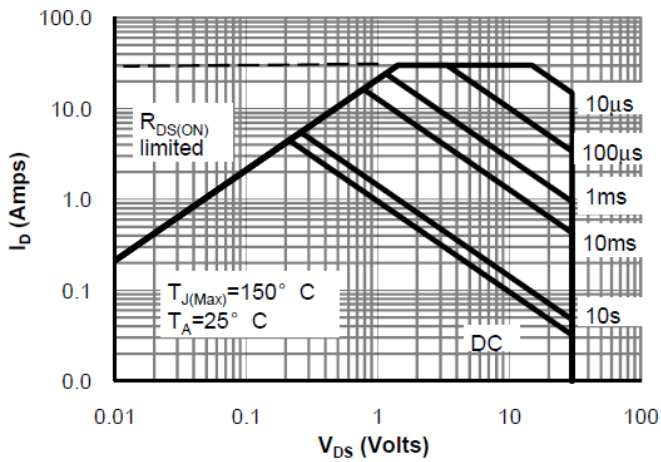


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

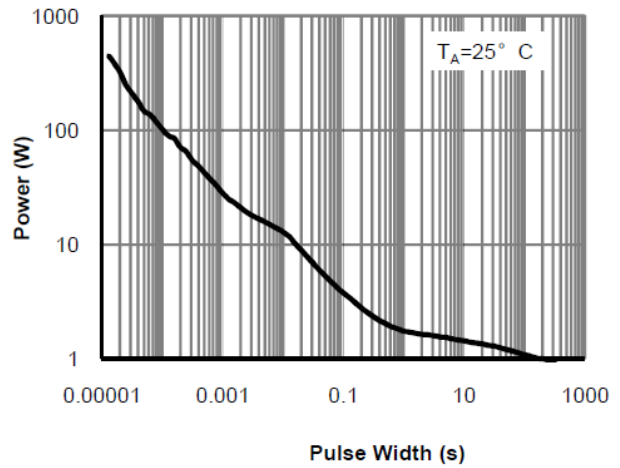


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

■ Typical Electrical and Thermal Characteristics

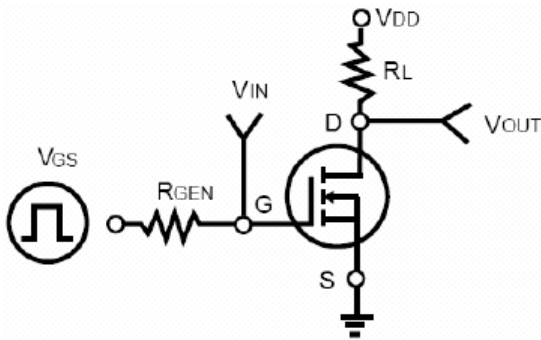


Figure 1: Switching Test Circuit

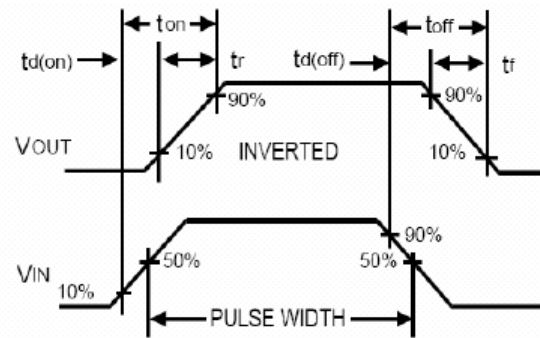


Figure 2: Switching Waveforms

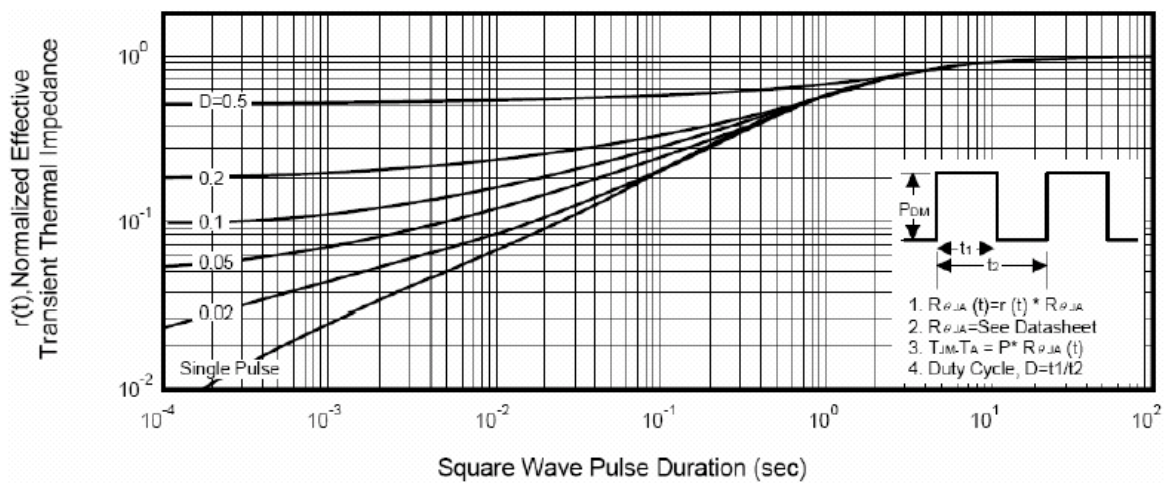
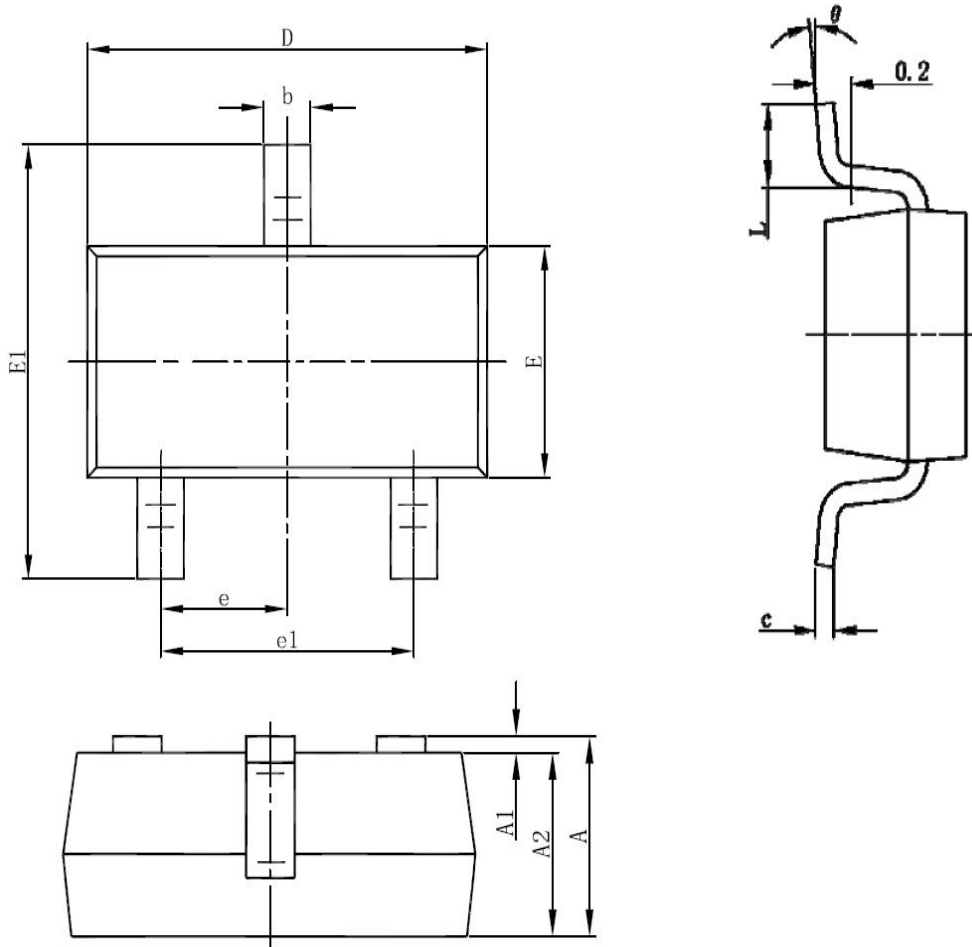


Figure 3: Normalized Maximum Transient Thermal Impedance

■ Package Dimensions : SOT-23-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°