

FH3050GS6

N-Channel Enhancement Mode Power MOSFET

Description

The FH3050GS6 uses advanced Shielded Gate trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

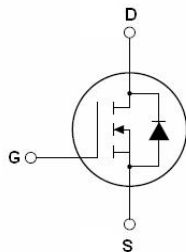
Application

- Motor drivers
- DC - DC Converter

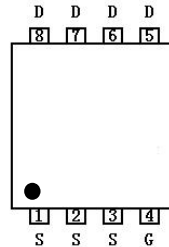
General Features

V_{DSS}	I_D	$R_{DS(ON)}$ (MAX)	
		$V_{GS}=10V$	$V_{GS}=4.5V$
30V	50A	6.5m Ω	9.5m Ω

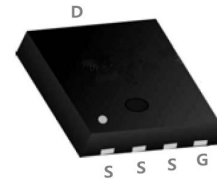
- Surface-mounted package
- Low Thermal Resistance



Schematic diagram



Marking and pin Assignment



PDFN3.3x3.3-8L top and bottom view

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	$T_c = 25^\circ\text{C}$	30	-	V
V_{GS}	Gate-Source Voltage	$T_c = 25^\circ\text{C}$	-	± 20	V
I_D^{***}	Drain Current	$T_c = 25^\circ\text{C}, V_{GS} = 10\text{V}$	-	50	A
I_{DM}^{*****}	Pulsed Source Current	$T_c = 25^\circ\text{C}, V_{GS} = 10\text{V}$	-	112	A
P_{tot}^*	Total Power Dissipation	$T_c = 25^\circ\text{C}$	-	20.8	W
T_{stg}	Storage Temperature		- 55	150	$^\circ\text{C}$
T_j	Junction Temperature		-	150	$^\circ\text{C}$
I_S	Diode Forward Current	$T_c = 25^\circ\text{C}$	-	50	A
$R_{\theta JA}^*$	Thermal Resistance- Junction to Ambient		-	62.5	$^\circ\text{C} / \text{W}$
$R_{\theta JC}^*$	Thermal Resistance- Junction to Case		-	6	

Notes :

- * Surface Mounted on 1 in² pad area, $t \leq 10$ sec
- ** Pulse width $\leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
- *** limited by bonding wire

Note: NHCX defines " Green " as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C)

Electrical Characteristics (TC=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250\ \mu\text{A}$	1.0	-	2.0	V
I_{DSS}	Zero Gate Voltage Source Current	$V_{DS} = 24, V_{GS} = 0\text{ V}$	-	-	1	μA
		$T_J = 85\text{ }^\circ\text{C}$	-	-	30	μA
I_{GSS}	Gate Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA
$R_{DS(ON)}^a$	Drain-Source On-State Resistance	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	-	5.8	6.5	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	-	8.9	9.5	
Diode Characteristics						
V_{SD}^a	Diode Forward Voltage	$I_{SD} = 20\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 20\text{ A}, dI_{SD}/dt = 100\text{ A}/\mu\text{s}$	-	23	-	nS
Q_{rr}	Reverse Recovery Charge		-	10	-	nC
Dynamic Characteristics^b						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}$ Frequency = 1 MHz	-	731	-	pF
C_{oss}	Output Capacitance		-	380	-	
C_{riss}	Reverse Transfer Capacitance		-	34	-	
$t_d(on)$	Turn-on Delay Time	$V_{DS} = 15\text{ V}, V_{GEN} = 10\text{ V},$ $R_G = 4.5\ \Omega, R_L = 0.75\ \Omega,$ $I_D = 20\text{ A}$	-	6.8	-	nS
t_r	Turn-on Rise Time		-	55	-	
$t_d(off)$	Turn-off Delay Time		-	12	-	
t_f	Turn-off Fall Time		-	20	-	
Gate Charge Characteristics^b						
Q_g	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $I_{DS} = 20\text{ A}$	-	14	-	nC
Q_{gs}	Gate-Source Charge		-	3.2	-	
Q_{gd}	Gate-Drain Charge		-	2.2	-	

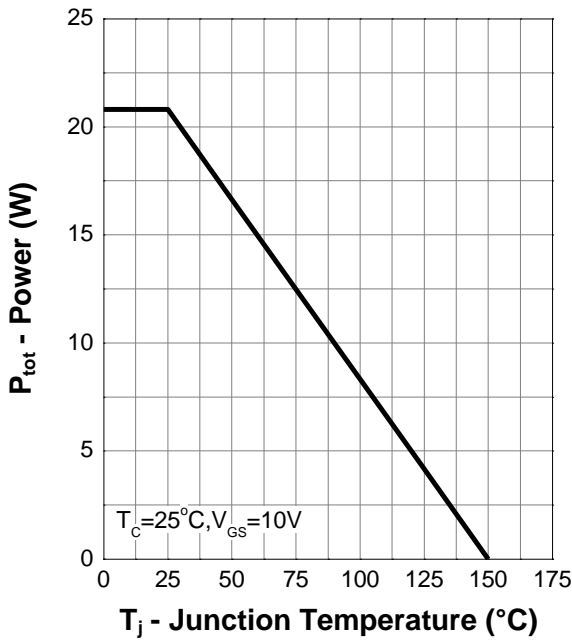
Notes :

a : Pulse test ; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

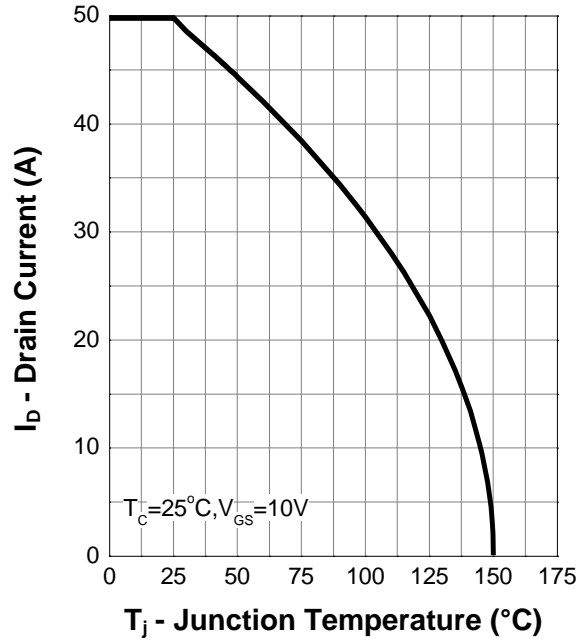
b : Guaranteed by design, not subject to production testing

Typical Characteristics (Cont.)

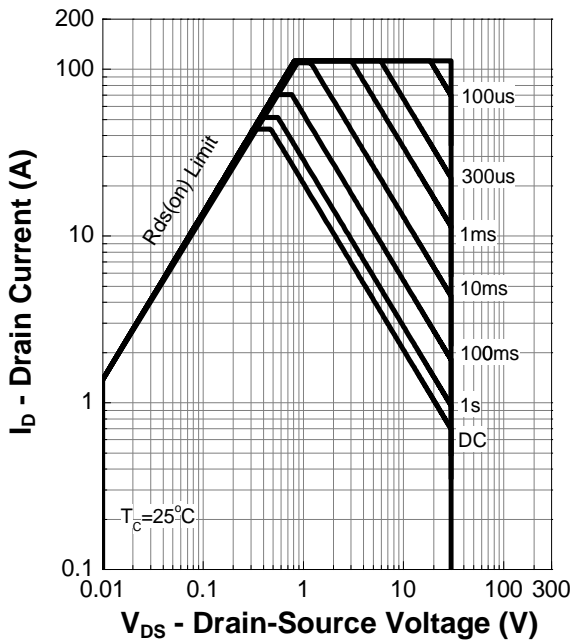
Power Capability



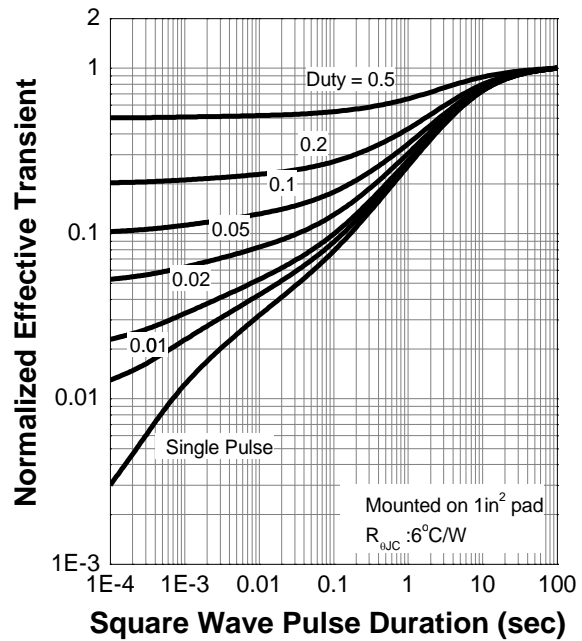
Current Capability



Safe Operating Area

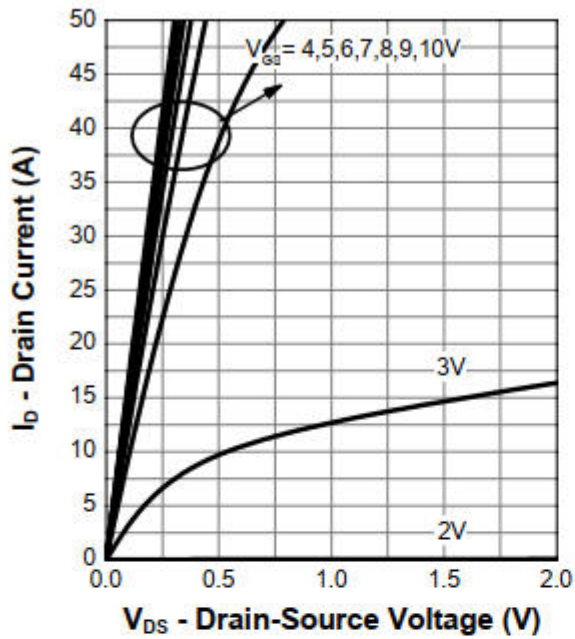


Transient Thermal Impedance

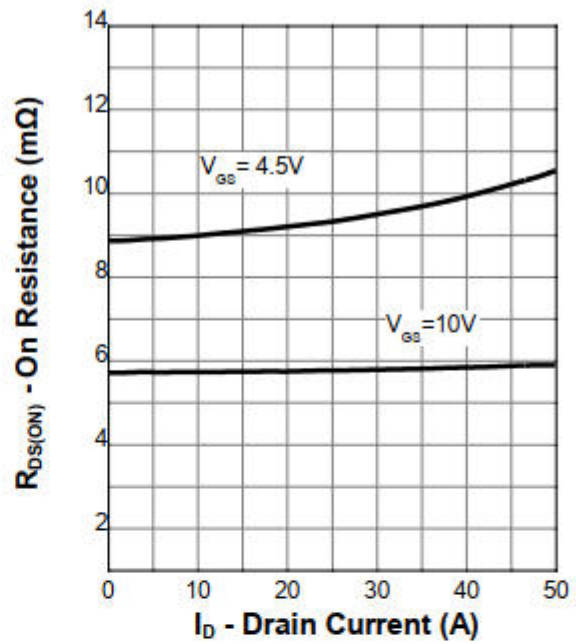


Typical Characteristics (Cont.)

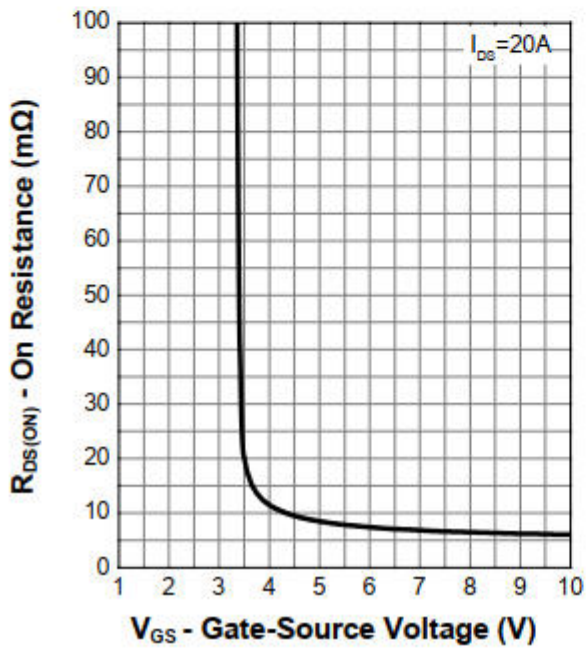
Output Characteristics



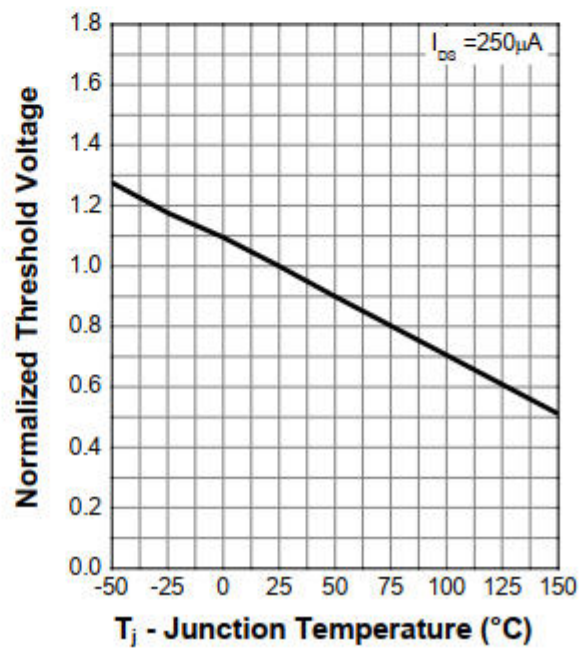
On Resistance



Transfer Characteristics

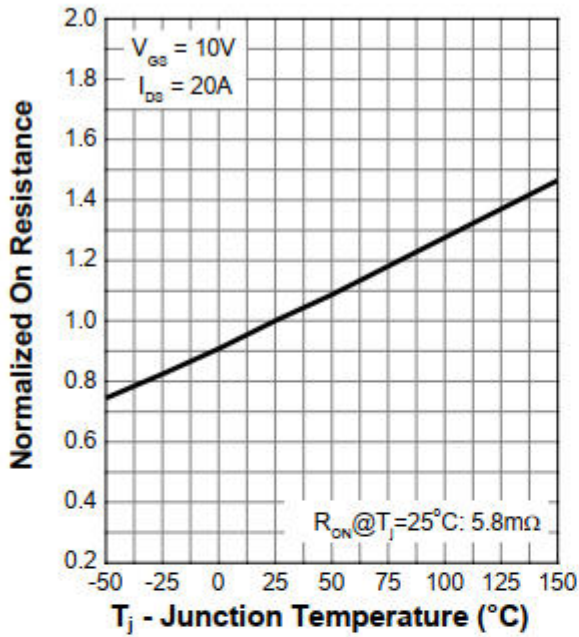


Normalized Threshold Voltage

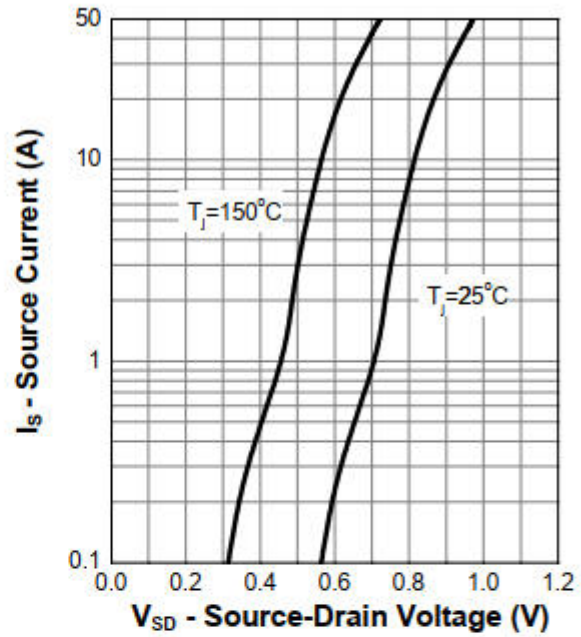


Typical Characteristics (Cont.)

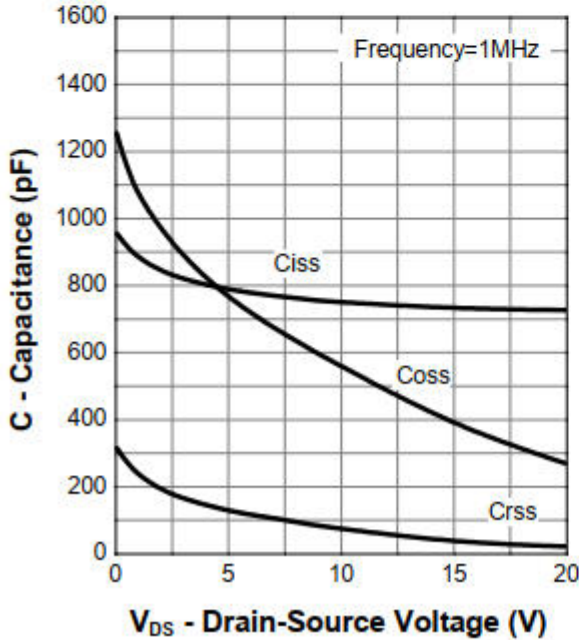
Normalized On Resistance



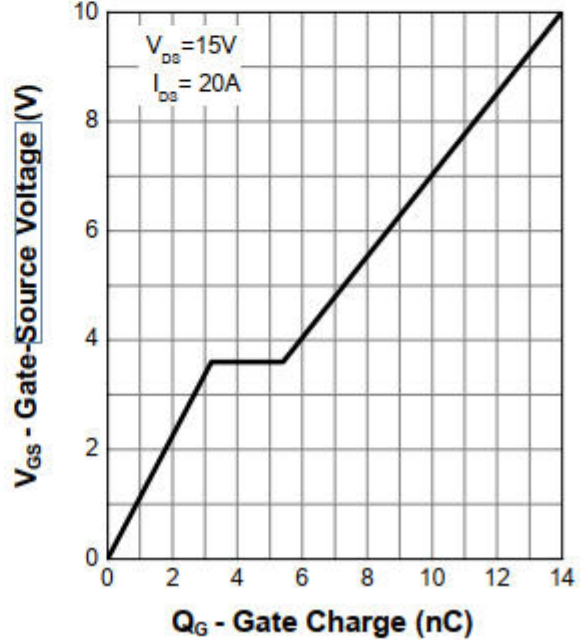
Diode Forward Current



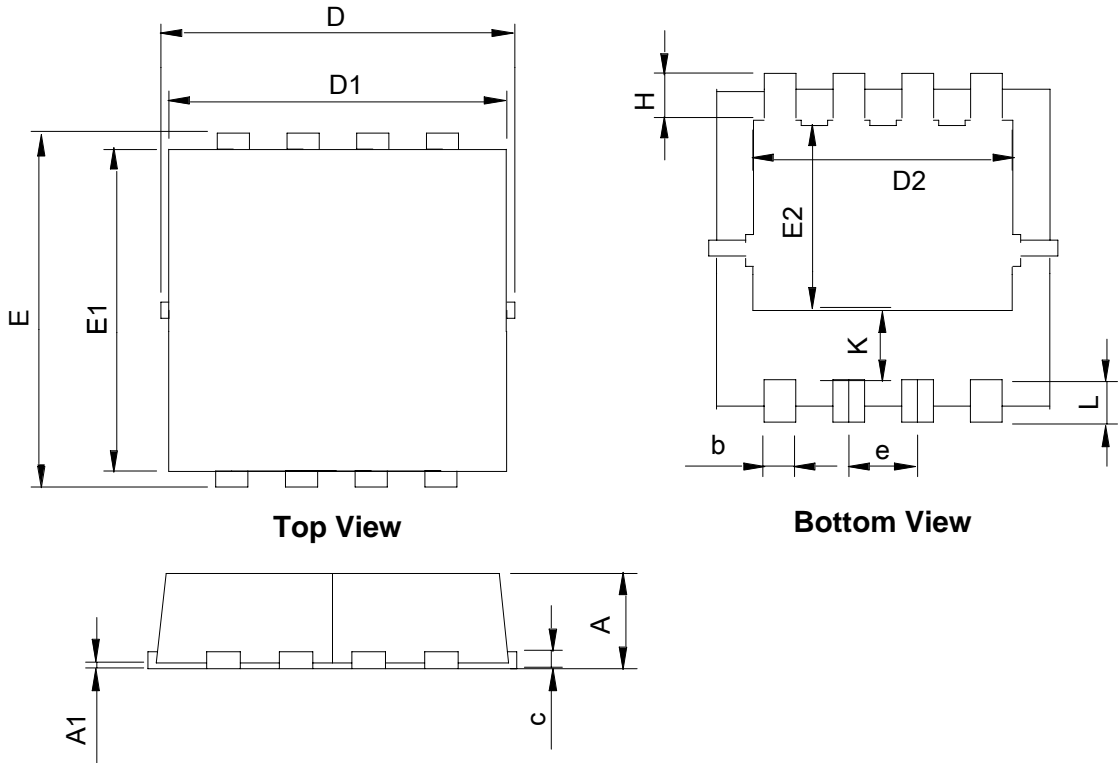
Capacitance



Gate Charge



Package Information : PDFN3.3x3.3-8L



SYMBOL	PDFN3.3x3.3-8L			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	1.00	0.028	0.039
A1	0.00	0.05	0.000	0.002
b	0.25	0.35	0.010	0.014
c	0.14	0.20	0.006	0.008
D	3.10	3.50	0.122	0.138
D1	3.05	3.25	0.120	0.128
D2	2.35	2.55	0.093	0.100
E	3.10	3.50	0.122	0.138
E1	2.90	3.10	0.114	0.122
E2	1.64	1.84	0.065	0.072
e	0.65 BSC		0.026 BSC	
H	0.32	0.52	0.013	0.020
K	0.59	0.79	0.023	0.031
L	0.25	0.55	0.010	0.022