

FH8838BG3

N- Channel Enhancement Mode Power MOSFET

Description

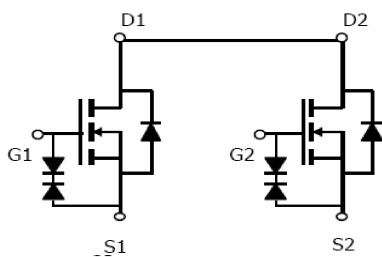
The FH8838BG3 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switch or in PWM applications. It is ESD protected.

Application

- PWM application
- Load switch

General Features

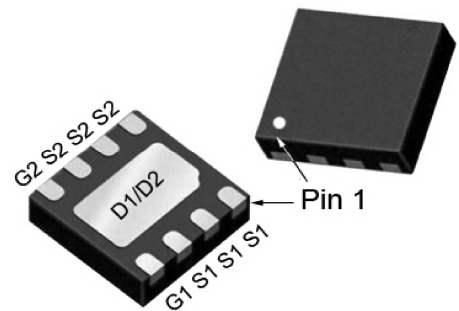
- $V_{DS} = 18V, I_D = 22A$
 $R_{DS(ON)} = 3.4 m\Omega$ (Typ) @ $V_{GS} = 4.5V$
 $R_{DS(ON)} = 3.6 m\Omega$ (Typ) @ $V_{GS} = 3.9V$
 $R_{DS(ON)} = 4.2 m\Omega$ (Typ) @ $V_{GS} = 2.5V$
- High Power and current handing capability
- Lead free product is acquired
- Surface Mount Package
- ESD Rating: 2000V HBM



Schematic diagram



Marking and pin assignment



DFN3x3-8L Pin assignment and Top / Bottom View

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	18	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current	$T_A = 25^\circ C$	I_D	22	A
	$T_A = 70^\circ C$		18	
Pulsed Drain Current (Note 1)		I_{DM}	88	
Avalanche Current		I_{AS}	22	
Avalanche Energy	$L = 0.1mH$	E_{AS}	29	mJ
Power Dissipation	$T_A = 25^\circ C$	P_D	3.7	W
	$T_A = 70^\circ C$		2.5	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	33.5	$^\circ C/W$
--	-----------------	------	--------------

Notes:

1. Pulse width limited by maximum junction temperature.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ C$.

Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	18	20	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 10V, V_{DS}=0V$	-	-	± 10	μA
On Characteristics (Note 2)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.45	0.80	1.20	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=8A$	2.0	3.4	4.4	m Ω
		$V_{GS}=3.9V, I_D=7A$	2.1	3.6	4.6	m Ω
		$V_{GS}=2.5V, I_D=6A$	3.0	4.2	5.5	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=5A$	-	40	-	S
Dynamic Characteristics (Note 3)						
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V,$ $F=1.0MHz$	-	3150	-	PF
Output Capacitance	C_{oss}		-	342	-	PF
Reverse Transfer Capacitance	C_{rss}		-	318	-	PF
Switching Characteristics (Note 3)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10V, R_L=1.35\Omega$ $V_{GS}=5V, R_{GEN}=3\Omega$	-	19		nS
Turn-on Rise Time	t_r		-	40		nS
Turn-Off Delay Time	$t_{d(off)}$		-	69		nS
Turn-Off Fall Time	t_f		-	16		nS
Total Gate Charge	Q_g	$V_{DS}=10V, I_D=7A,$ $V_{GS}=4.5V$	-	35		nC
Gate-Source Charge	Q_{gs}		-	3	-	nC
Gate-Drain Charge	Q_{gd}		-	10	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 2)	V_{SD}	$V_{GS}=0V, I_S=1A$	-	-	1.3	V
Diode Forward Current (Note 1)	I_S		-	-	22	A

Notes:

1. Surface Mounted on FR4 Board, $t \leq 10$ sec.
2. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
3. Guaranteed by design, not subject to production

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

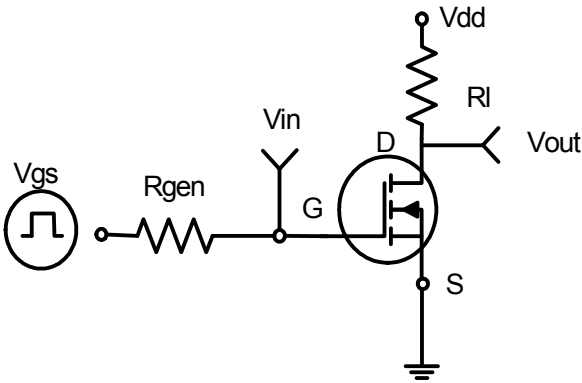


Figure 1: Switching Test Circuit

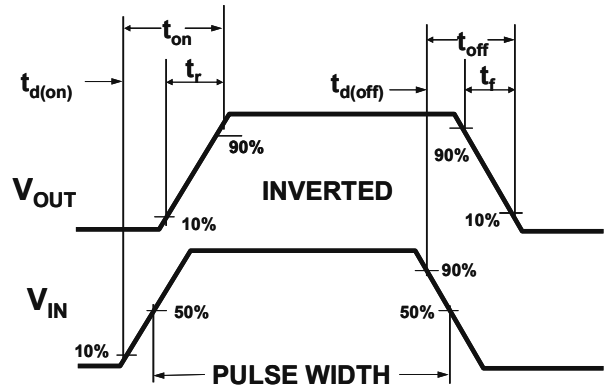


Figure 2: Switching Waveforms

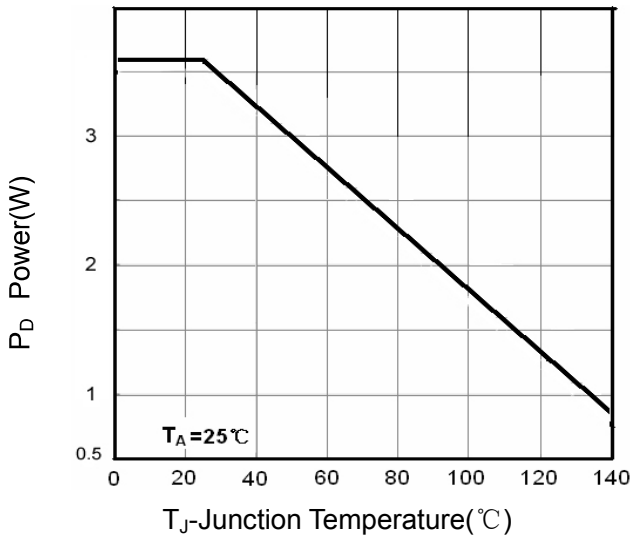


Figure 3 Power Dissipation

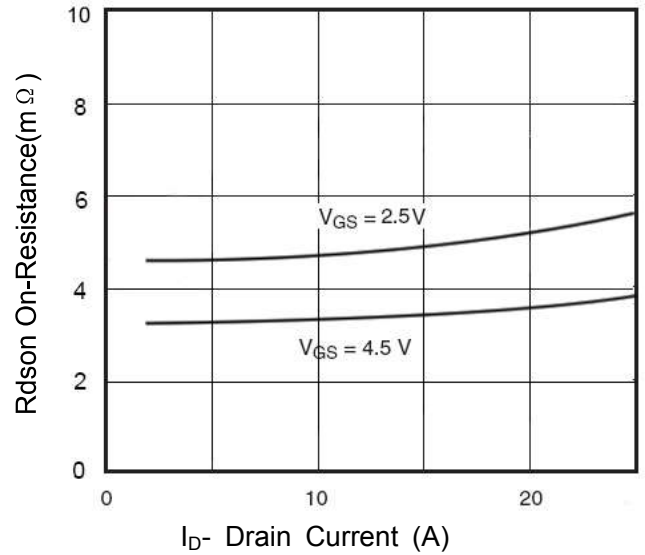


Figure 4 Drain-Source On-Resistance

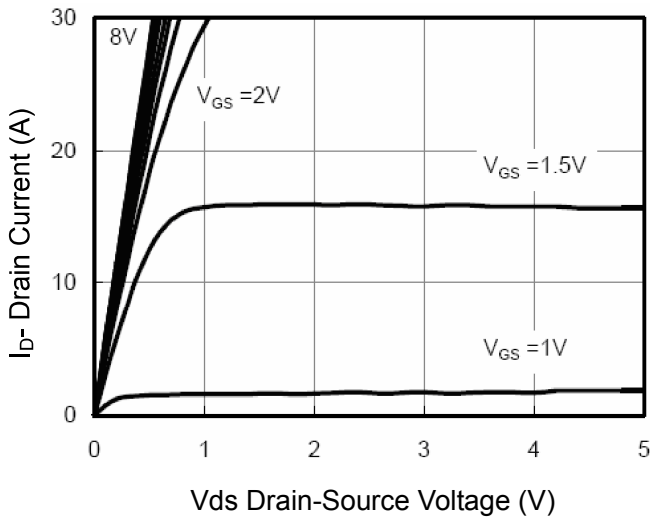


Figure 5 Output CHARACTERISTICS

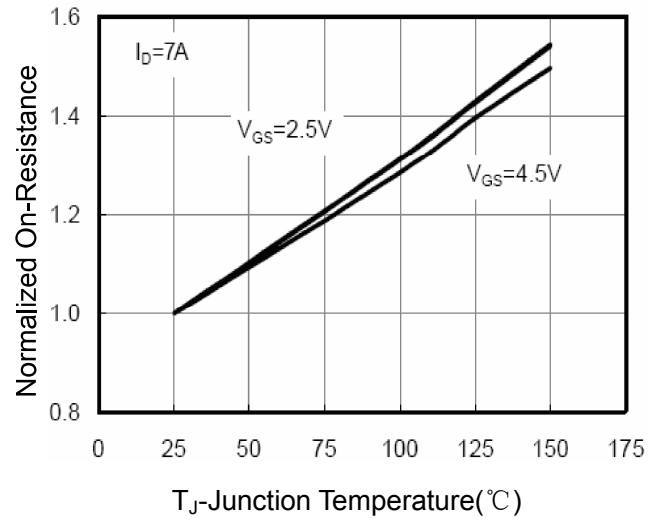
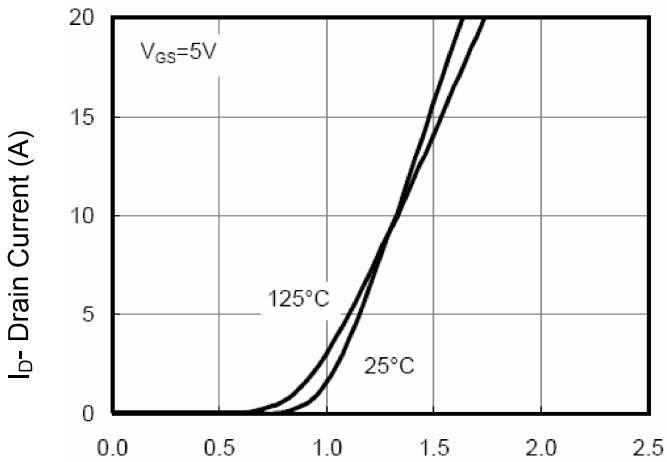
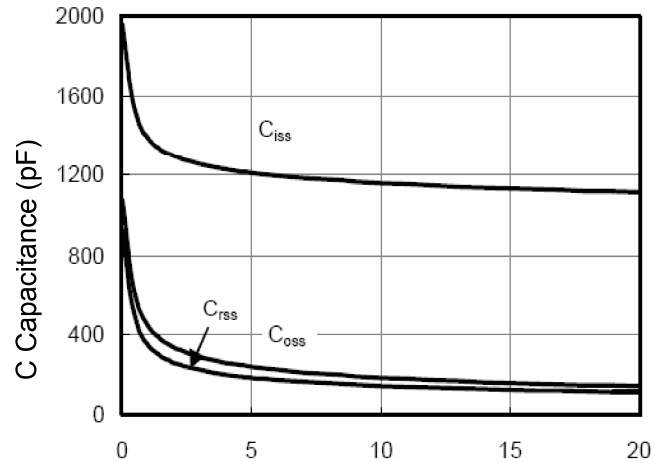


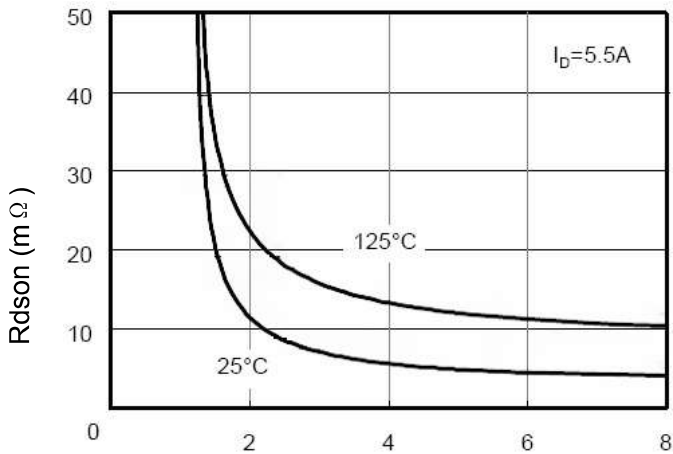
Figure 6 Drain-Source On-Resistance



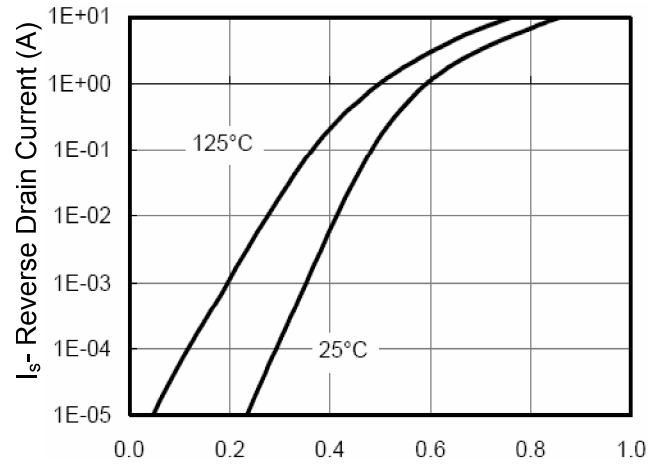
Vgs Gate-Source Voltage (V)
Figure 7 Transfer Characteristics



Vds Drain-Source Voltage (V)
Figure 8 Capacitance vs Vds



Vgs Gate-Source Voltage (V)
Figure 9 Rdson vs Vgs



Vds Drain-Source Voltage (V)
Figure 10 Capacitance vs Vds

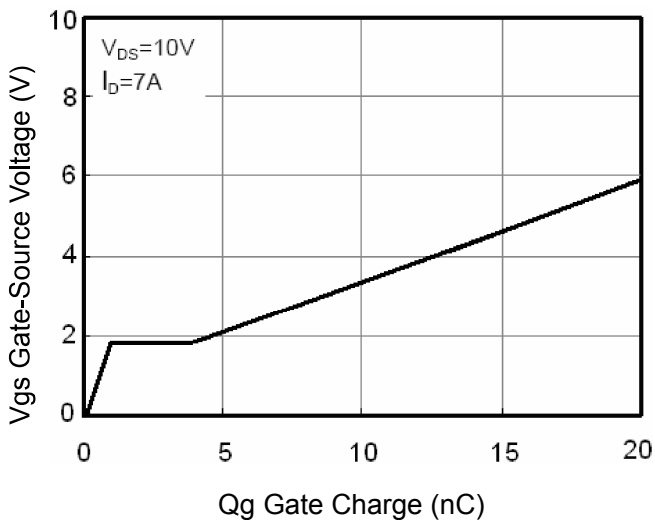


Figure 11 Gate Charge

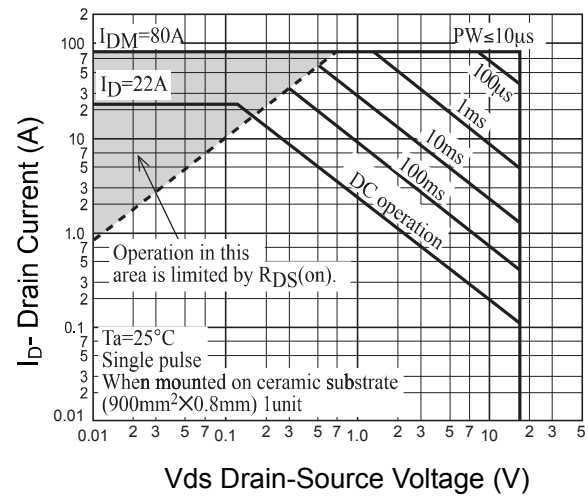


Figure 12 Safe Operation Area

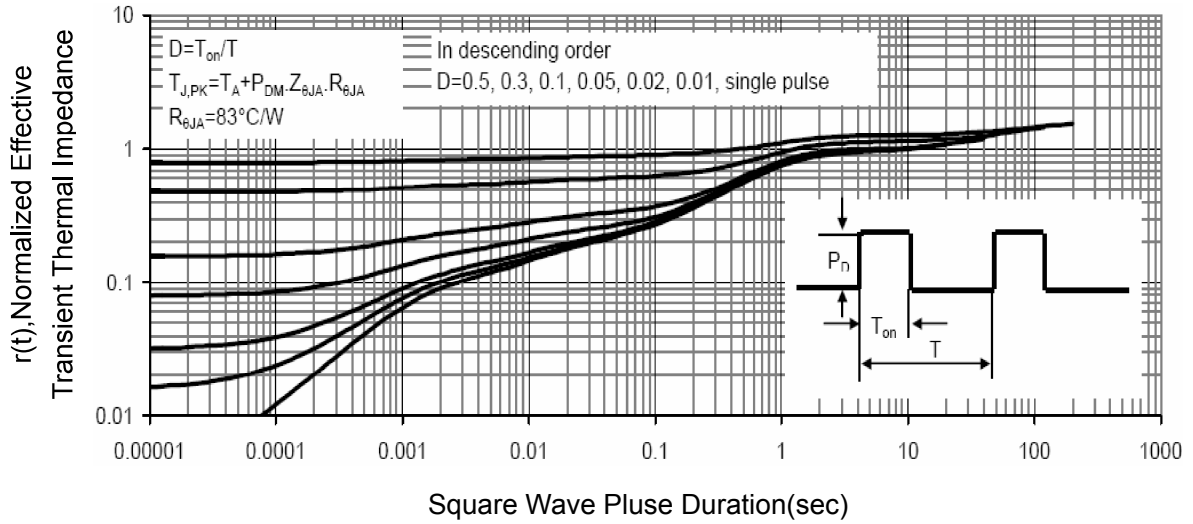
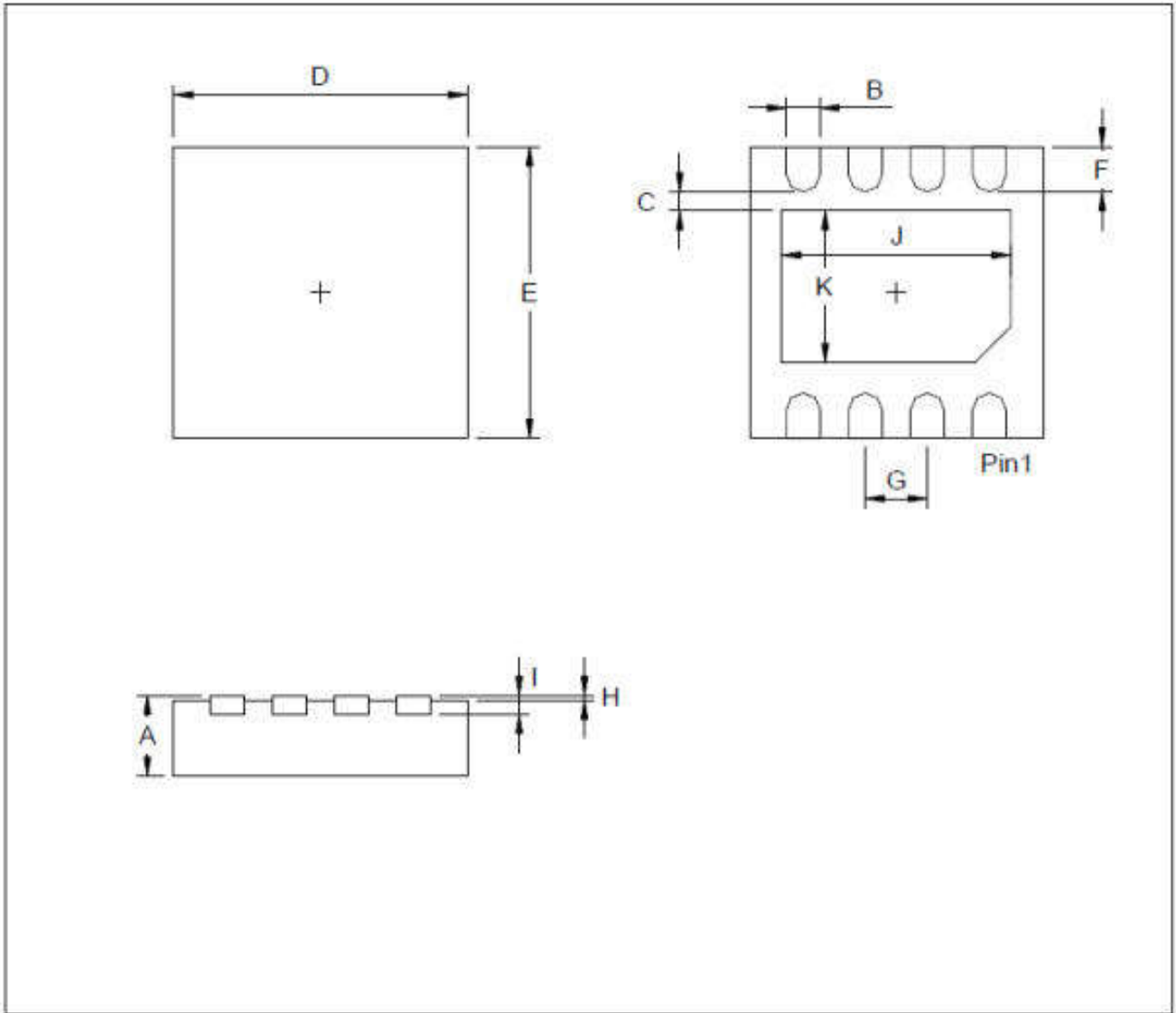


Figure 13 Normalized Maximum Transient Thermal Impedance

Package Outline Dimensions : DFN3*3-8L



Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	0.7		0.8	I		0.203	
B	0.25		0.35	J	2.2		2.4
C	0.2			K	1.4		1.6
D	2.924		3.076				
E	2.924		3.076				
F	0.324		0.476				
G		0.65					
H	0		0.05				